DATASHEET

VT-DRM(S)

DIGITAL RADFET READOUT MODULE

DESCRIPTION

Designed in partnership with the European Space Agency (ESA), VT- DRM(S) is a total ionizing dose (TID) measuring module aimed at providing an optimized RADFET read-out for various RADFET technologies. The VT-DRM(S) utilizes 100 nm and 400 nm RADFETs in various sense modes, covering both read-out and irradiation (sense) mode.

The module outputs a digitized threshold voltage, which is directly related to accumulated radiation dose. Designed to compensate for threshold voltage drift due to temperature, VT-DRM(S) provides a stable readout over a large temperature span. VT-DRM(S) can be easily integrated with the host. VT-DRM(S) communicates with the host via standard SPI protocol or isoSPI.

Available Q4 2024.

KEY FEATURES

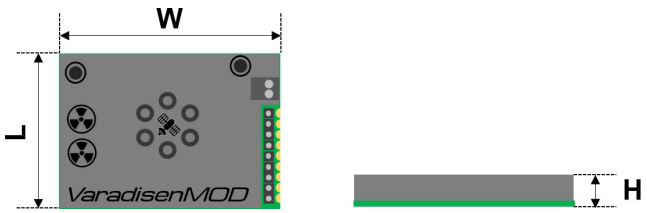
- Comprises two 400 nm RADFETs and two 100 nm RADFETs
- Temperature endurance range: -40°C to +85°C
- Onboard temperature sensor
- Maximum sensitivity: 130 mV/Gy
- Dimensions: 35 mm x 50 mm x 7 mm
- Communication: Standard SPI or isoSPI on distance up to 100 m

TYPICAL APPLICATIONS

- Satellites
- Accelerator facilities
- Nuclear power stations
- General purpose radiation detection

CONNECTOR ASSIGNMENT AND DIMENSIONS

VT-DRM(S) connector assignment and PCB outline drawing are provided in Figure 1, with the pin description in Table 1.



Parameter	Min	Typical	Max
Width	-	50 mm	-
Length	-	35 mm	-
Height	-	7 mm	10 mm
Weight	10 g	TBM	TBM

Figure 1: VT-DRM(S) connector assignment and PCB outline drawing and dimensions

Table 1: Pin description

NO.	PIN NAME	PIN TYPE	DESCRIPTION / RECOMMENDATIONS
1	Va	POWER	Analog positive power supply, this pin must be decoupled with 10 µF ceramic, low ESR capacitor
2	Vdd	POWER	Digital positive power supply, this pin must be decoupled with 10 µF ceramic, low ESR capacitor
3	GND	GND	Connect to power supply ground
4	Din	Digital IN	Serial Data Input
5	CS	Digital IN	Chip select; active low
6	DOUT	Digital OUT	Serial data output combined with data ready; active low
7	SYNC	Digital IN	Start conversion
8	SCLK	Digital IN	Serial clock input
9	GND	GND	Connect to power supply ground
isoSPI	Im	Analog In/out	Isolated Interface Minus Input/Output
isoSPI	Pp	Analog In/out	Isolated Interface Plus Input/Output

BLOCK DIAGRAM

The schematic diagram of the VT-DRM(S) module is shown in Figure 2.

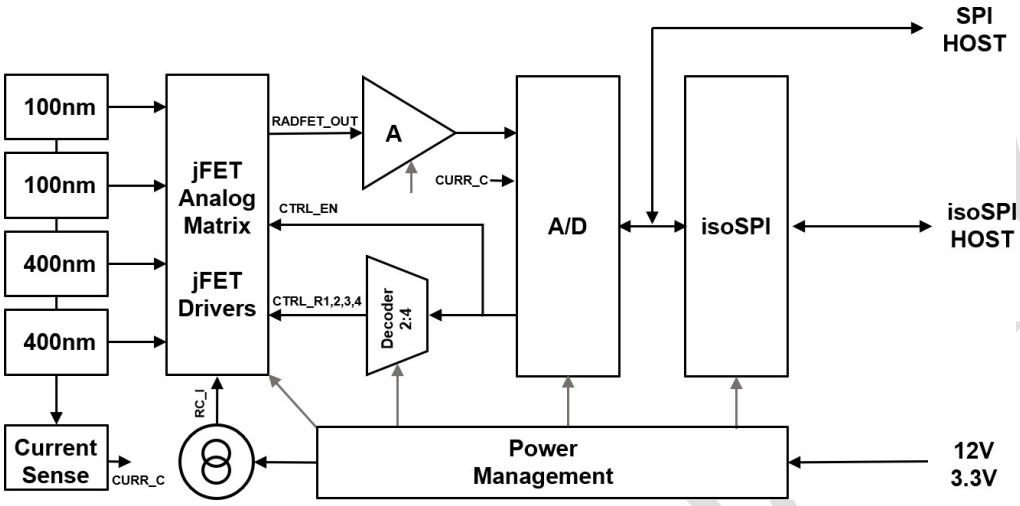


Figure 2: VT-DRM(S) schematic diagram

OPERATION PRINCIPLE

The main sensing elements of the VT-DRM(S) readout module are the RADFET parts, in two oxide thickness variants of 100 nm and 400 nm; thus, two different sensitivities. Each RADFET part consists of two identical transistors, R1 and R2, and a diode. The VT-DRM(S) can be irradiated in active (powered) and passive (unpowered, Va=Vdd=0V) mode. Irradiation (sense) and Read-out modes are implemented by a series of analog switches (j-FETs), providing appropriate biasing conditions.

READ-OUT MODE (ACCUMULATED RADIATION DOSE READ-OUT)

Readout mode (RADFET selection) is set by control signals CTRL_EN, CTRL_R1,2,3,4 generated from the ADC. In Irradiation mode, all RADFET terminals are grounded. In Read-out mode, the selected RADFET is biased in Reader Circuit configuration–Drain/Gate tied together and grounded, Source/Bulk tied together, constant DC current source connected to Source/Bulk, RADFET Reader Circuit threshold voltage (RC_V = VTH) read at Source/Bulk.

The current source on VT-DRM(S) is optimized for stability and its current level RC_I to minimize temperature drift. The VTH signal is multiplexed, buffered, and filtered, available at (RADFET_OUT) for digitalization by the ADC.

The device may be read at arbitrary intervals, depending on the application. The period between readings should be from seconds to days or even months. The circuit used to read out the chip should be similar to the circuit shown below and should be read in connection with the configuration table.

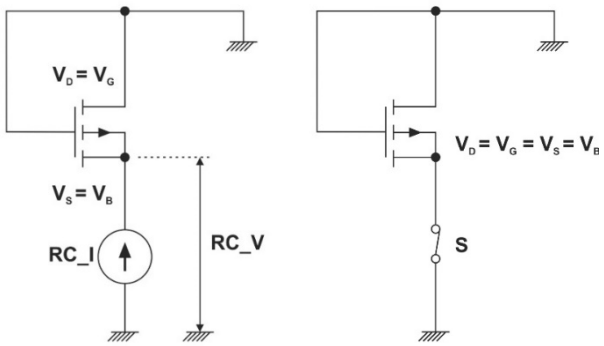


Figure 3: VT-DRM(S) rider circuit configuration

IRRADIATION MODE (SENSE MODE)

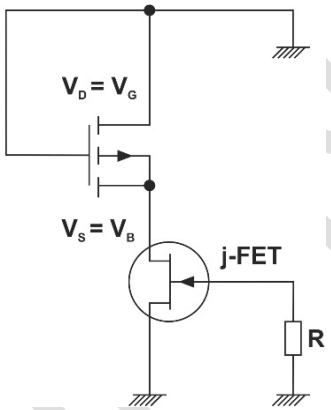


Figure 4: VT-DRM(S) zero bias during irradiation (sense mode)

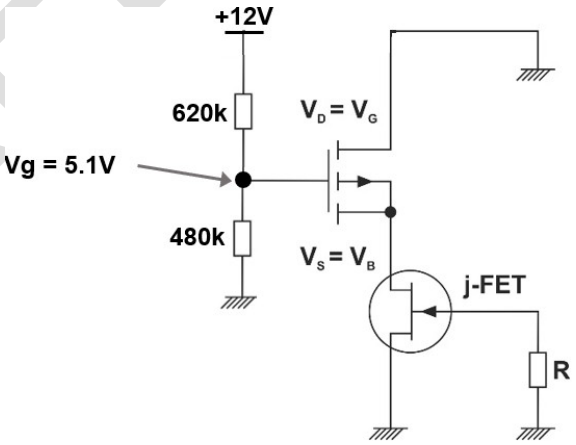


Figure 5: VT-DRM(S) +Vg bias during irradiation (sense mode)

RADFET OUTPUT VALUES AND TIMING

The main component responsible for communication with the host is the SPI interface of the ADS124S06 analog to digital converter. The ADS124S06 has a three-wire or four-wire SPI interface that is compatible with various DSP units.

The SPI-compatible serial interface is used to read the conversion data and to configure and control the ADC. The serial interface consists of four signals: CS, SCLK, DIN, and DOUT/DRDY. The conversion data are provided with an optional CRC code for improved data integrity. The dual function DOUT/DRDY output indicates when conversion data are ready and provides the data output. The serial interface can be implemented with as little as three connections by tying CS low. Start ADC conversions with either the START/SYNC pin or with commands. The ADC can be programmed for a continuous conversion mode or to perform single-shot conversions.

The module can be configured in different read-out/conversion modes, more details in the following figures:

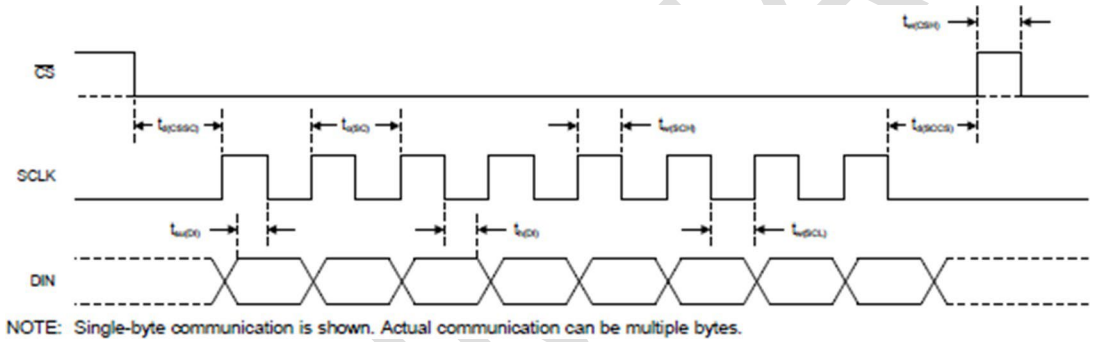


Figure 6: Interface Timing Requirements

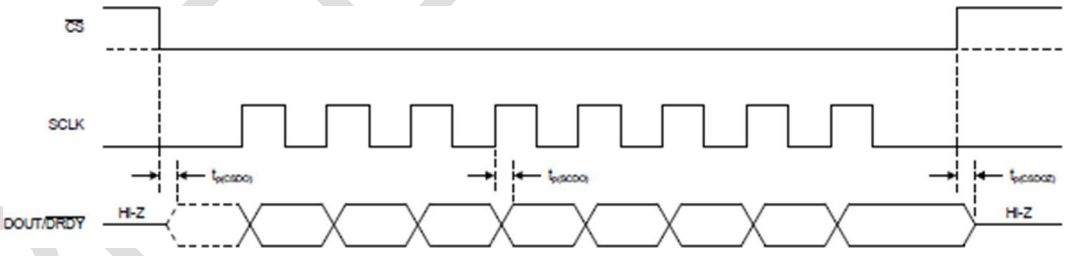


Figure 7: Serial Interface Switching Characteristics

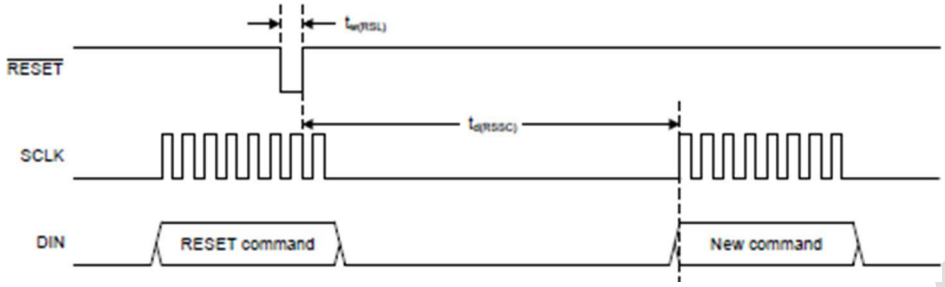


Figure 8: RESET Pin and RESET Command Timing Requirements

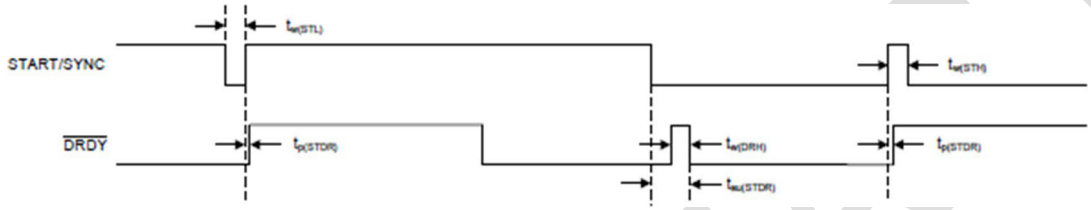


Figure 9: START/SYNC Pin Timing Requirements

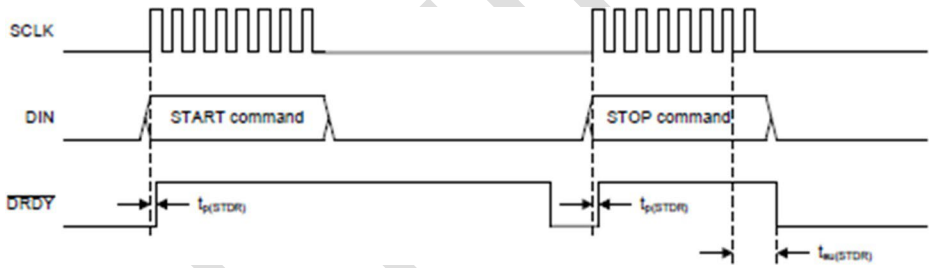


Figure 10: START Command Timing Requirements

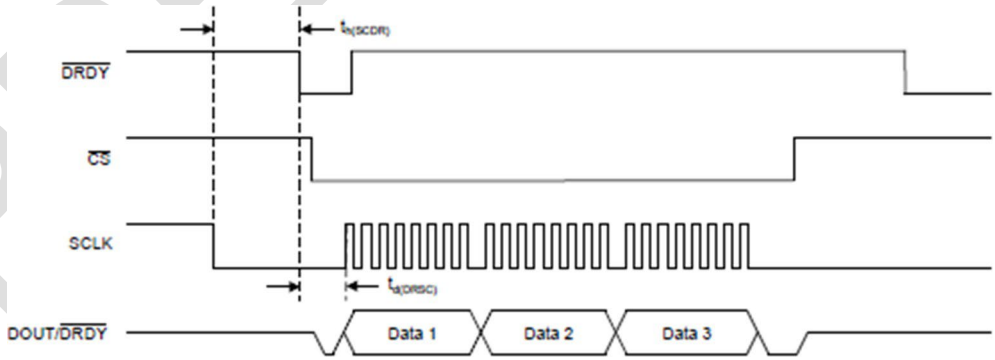


Figure 11: Read Data Direct (Without an RDATA Command) Timing Requirements

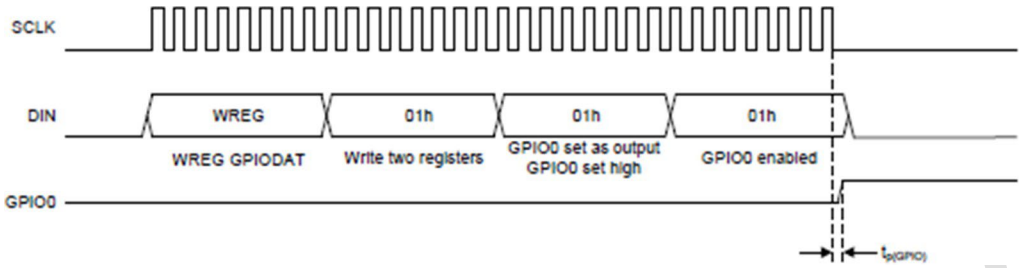


Figure 12: GPIO Switching Characteristics

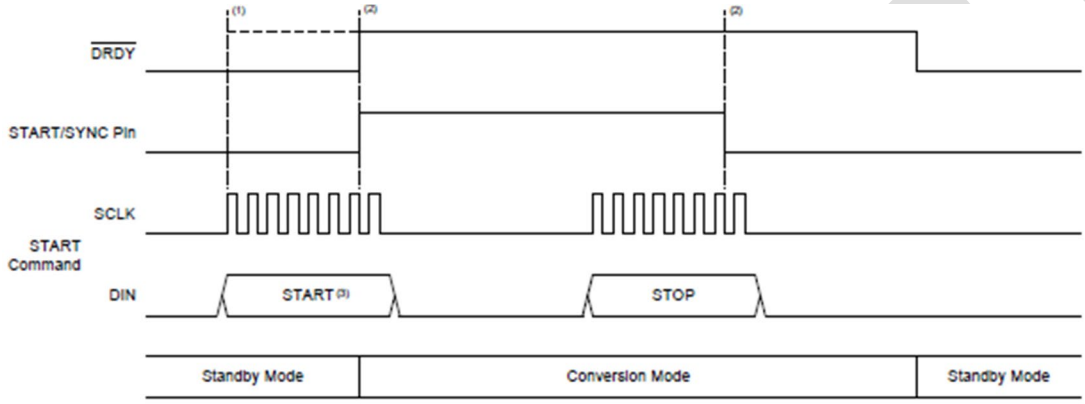


Figure 13: Conversion Start and Stop Timing

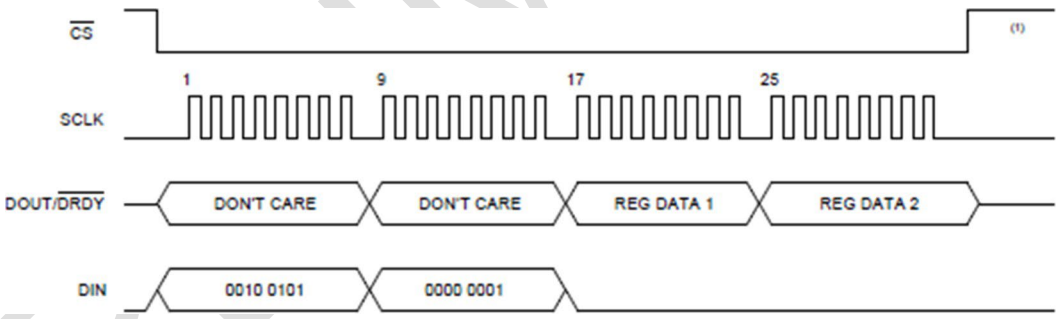


Figure 14: Read Register Sequence

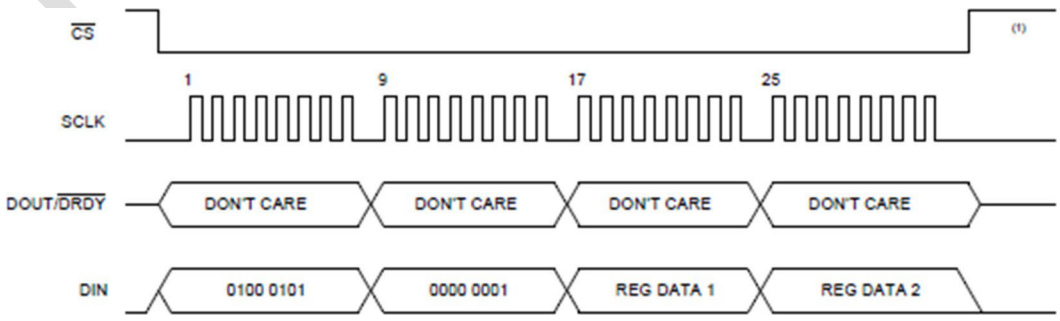


Figure 15: Write Register Sequence

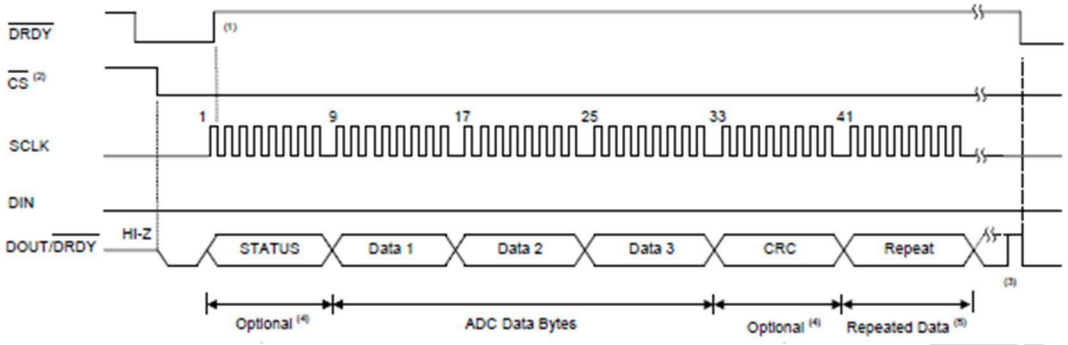


Figure 16: Read Data Direct

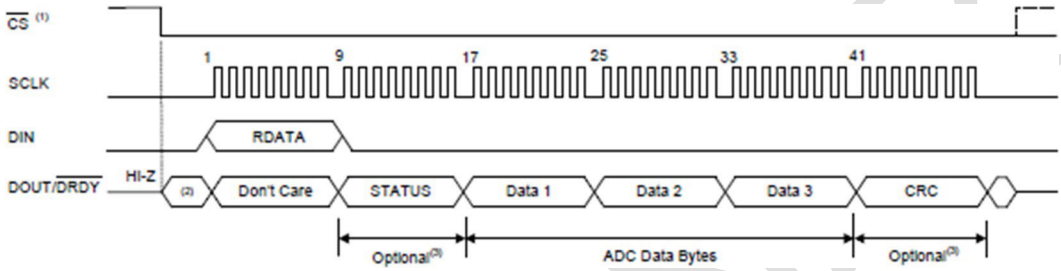


Figure 17: Read Data by Command

The isoSPI communication is established by the LTC6820 chip which provides bidirectional SPI communications between two isolated devices through a single twisted pair connection. Each LTC6820 encodes logic states into signals that are transmitted across an isolation barrier to another LTC6820.

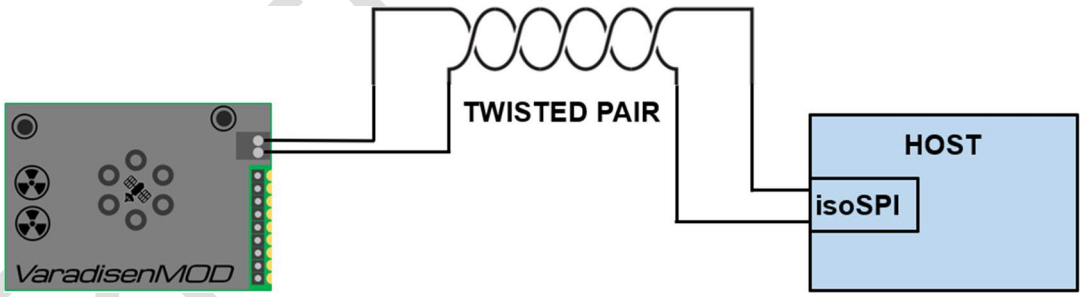


Figure 18: isoSPI connection with HOST

RADIATION CALIBRATION DATA

TID up to 50 Gy (5 kRad)

Contact support@varadis.com for more details.

RECOMMENDED OPERATING CONDITIONS

VT-DRM(S) module recommended operating conditions are provided in Table 4.

Table 2: Recommended Operating Conditions

SYMBOL	PARAMETER	VALUE	UNIT
Vdd	Supply voltage, referenced to GND	3.3 V	V
Va	Supply voltage, referenced to GND	12 V	V
Din	Serial Data Input	Vdd-0.2	V
CS	Chip Select Input	Vdd-0.2	V
DOUT	Serial Data Output/Data Ready Output	Vdd-0.2	V
SYNC	Synchronization Input	Vdd-0.2	V
SCLK	Serial Data Input to the Input Shift Register on the module	Vdd-0.2	V
GND	Supply ground	0	V
Im	Isolated Interface Minus Input/Output	-	V
Pp	Isolated Interface Plus Input/Output	-	V
T	Ambient operating temperature	22	ºC
ARH	Ambient relative humidity (non-condensed)	< 85	%

DC Electrical Characteristics

VT-DRM(S) module DC electrical characteristics are given in Table 3.

Table 3: DC electrical characteristics

PARAMETER	MIN	TYPICAL	MAX
Digital supply	2.7 V	3.3 V	3.6 V
Analog supply	11 V	12 V	15 V
Current consumption reading mode	0	5 mA	10 mA
Current consumption sense mode	0[1]	100 nA	30 uA
Sensitivity[2] 100 nm Zero Biased		1.5 mV/Gy	
Sensitivity 100 nm +Gate Biased		5.96 mV/Gy	
Sensitivity 400 nm Zero Biased		0.55 mV/cGy	
Sensitivity 400nm +Gate Biased		130 mV/Gy	
Total ionizing dose	1 cGy		1kGy
Temperature range	-55°C	20°C	85°C
Measurement interval	15 sec	2 min	1 day

[1] In case of unpowered module, when Va=Vdd=0V

[2] The sensitivity decreases with the received dose, the given typical sensitivity is extracted from the linear region (beginning of radiation)

isoSPI DEMO CIRCUIT INTERFACE

In the following diagram a demo connection with a host using development kits DC1941D isoSPI™ Demo Board and DC2026C, Linduino One Isolated Arduino-Compatible Demonstration Board:

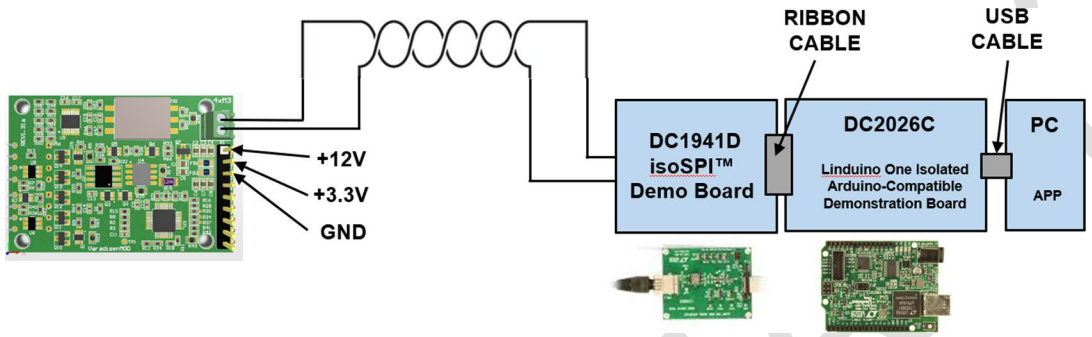


Figure 19: isoSPI example connection with PC

SOLDERING AND MOUNTING

It is important that the VT-DRM(S) is the last component to be hand soldered onto a circuit board. If a different soldering profile is required, please contact us at support@varadis.com.

VT-DRM(S) can be soldered directly on the customer PCB (treated as SMD) or via standard through hole 10-pin header connector with a pitch of 2.54 mm; example (Mfr. No: 1-826629- 0). Recommended dimensions for solder pad layout are given in Figure 7.

HANDLING

All assembled boards undergo 100% electrical test and visual inspection immediately prior to shipment. Therefore, all boards should reach the customer in excellent condition. To ensure that the boards remain in this condition, please handle the parts as carefully as possible and observe standard precautions related to ESD sensitive devices.

NOTES

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