

TECHNICAL DATA

VT-DRM(S)

Digital RADFET Readout Module

Multiple RADFET technologies

Hermetically Sealed Ceramic Package

For doses between 1cGy(1Rad) and 150Gy(15kRad)



Features

- Comprises:
 - two 400 nm RADFETs
 - two 100 nm RADFETs
- Temperature endurance range:
-40°C to +85°C
- Onboard temperature sensor
- Maximal sensitivity: 130 mV/Gy
- Dimensions: 39 mm x 53 mm x 8.5 mm
- Communication:
 - SPI
 - isoSPI on distance up to 100 m

Description

Built to meet European Space Agency (ESA) standards, VT-DRM(S) is a total ionizing dose (TID) measuring module aimed at providing an optimized RADFET read-out for various RADFET technologies. The VT-DRM(S) utilizes 100 nm and 400 nm RADFETs in various sense modes, covering both read-out and irradiation (sense) mode. The module outputs a digitized threshold voltage, which is directly related to accumulated radiation dose. Designed to compensate for threshold voltage drift due to temperature, VT-DRM(S) provides a stable readout over a large temperature span. VT-DRM(S) can be easily integrated with the host. VT-DRM(S) communicates with the host via standard SPI protocol or isoSPI.

Typical applications

- Space/Satellite Safety
- Smart City/Public Safety
- Prompt dose dosimetry
- Accelerator facilities
- Nuclear power stations
- General purpose radiation detection

Pin Assignment and Dimensions

VT-DRM(S) pin assignment and PCB outline drawing are given in Figure 1 and Table 2, while dimensions details are given in Table 1.

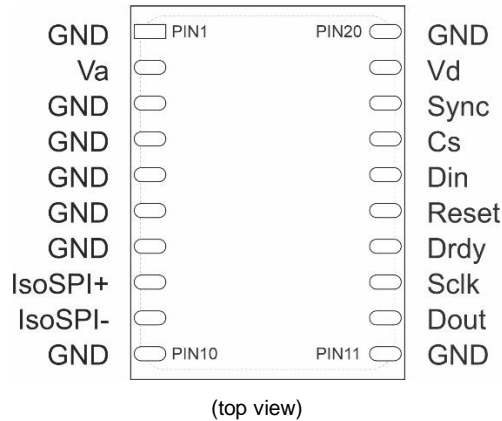


Table 1: VT-DRM(S) dimensions description

| Parameter | Min | Typical | Max |
|-----------|-----|---------|-----|
| Width | - | 53mm | - |
| Length | - | 39mm | - |
| Height | - | 8.5mm | - |
| Weight | 20g | - | - |



Figure 1 VT-DRM(S) pin assignment, outline drawing and dimensions.

Table 2: Pin description

| No. | Pin name | Pin type | Description / Recommendations |
|--------|----------|-------------|---|
| 1 | GND | GND | Connect to power supply ground. |
| 2 | Va | POWER | Analog positive power supply, this pin must be decoupled with 10 μ F ceramic, low ESR capacitor. |
| 3 to 7 | GND | GND | Connect to power supply ground. |
| 8 | Pp | isoSPI | Isolated Interface Plus Input/Output |
| 9 | Im | isoSPI | Isolated Interface Minus Input/Output. |
| 10, 11 | GND | GND | Connect to power supply ground. |
| 12 | DOUT | Digital OUT | Serial data output combined with data ready |
| 13 | SCLK | Digital IN | Serial clock input |
| 14 | DRDY | Digital OUT | Data ready |
| 15 | RESET | Digital OUT | Module ADC reset pin |
| 16 | Din | Digital IN | Serial Data Input |
| 17 | CS | Digital IN | Chip select |
| 18 | SYNC | Digital IN | Start conversion |
| 19 | Vdd | POWER | Digital positive power supply, this pin must be decoupled with 10 μ F ceramic, low ESR capacitor. |
| 20 | GND | GND | Connect to power supply ground. |

Block Diagram

The schematic block diagram of the VT-DRM(S) module is shown in Figure 2.

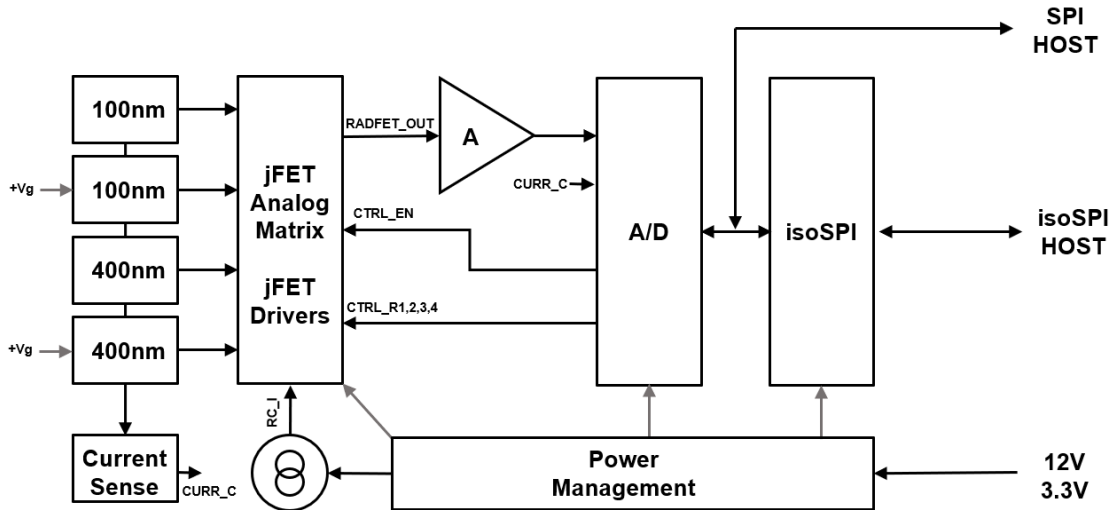


Figure 2: VT-DRM(S) schematic block diagram.

Operation Principle

The main sensing elements of the VT-DRM(S) module are two RADFET parts, with oxide thickness of 100nm and 400nm. Each RADFET consists of two identical transistors, R1 and R2. The readout selection of the RADFETs is set by control signals CTRL_EN, CTRL_R1,2,3,4 generated by the ADC. In readout mode, the selected RADFET is biased in Reader Circuit configuration – Drain/Gate tied together and grounded, Source/Bulk tied together, while constant DC current source is connected to the Source/Bulk. The reader circuit voltage (RC_V) is equal to the threshold voltage of the RADFET (V_{TH}) read at Source/Bulk, see details in Figure 3.

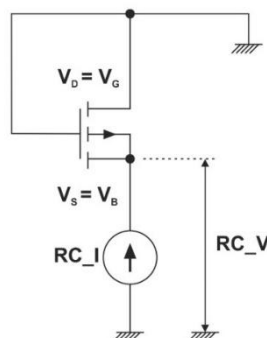


Figure 3: RADFET rider circuit configuration.

During sensing R1 is zero biased while R2 is +Vg biased, Figure 4 and 5.

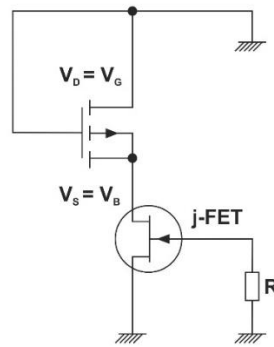


Figure 4 RADFET zero bias during irradiation (sense mode)

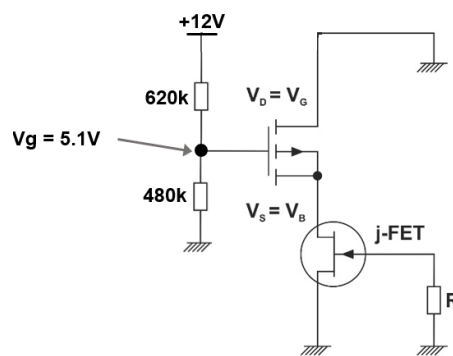


Figure 5: RADFET +Vg bias during irradiation (sense mode)

The current source is optimized for stability and its current level RC_I to minimize temperature drift. The V_{TH} signal is multiplexed, buffered, filtered, and digitalised by the ADC. The digitalised V_{th} value can be converted into accumulated dose using calibration parameters provided by Varadis.

The module is equipped with onboard temperature sensor (Thermistor), which data can be accessed through the ADC using specific commands. In some cases, where wide span of temperatures is present, the temp data can be used for correction of the RADFET's data.

The VT-DRM(S) can be used in active or passive mode, the device may be read at arbitrary intervals, depending on the application. The period between readings can be from seconds to days or even months. Please contact support@varadis.com for more details.

Module Output Values and Timing

The main component responsible for communication with the HOST is the SPI interface of the ADS124S06 analog to digital converter. The ADS124S06 has a 3-wire or 4-wire SPI interface that is compatible with various DSP units.

The SPI-compatible serial interface is used to read the conversion data and also to configure and control the ADC. The serial interface consists of four signals: CS, SCLK, DIN, and DOUT/DRDY. The conversion data is provided with an optional CRC code for improved data integrity. The dual function DOUT/DRDY output indicates when conversion data is ready and also provides the data output. The serial interface can be implemented with as little as three connections by tying CS low. Start ADC conversions with either the START/SYNC pin or with commands. The ADC can be programmed for a continuous conversion mode or to perform single-shot conversions. More details in the following Figures:

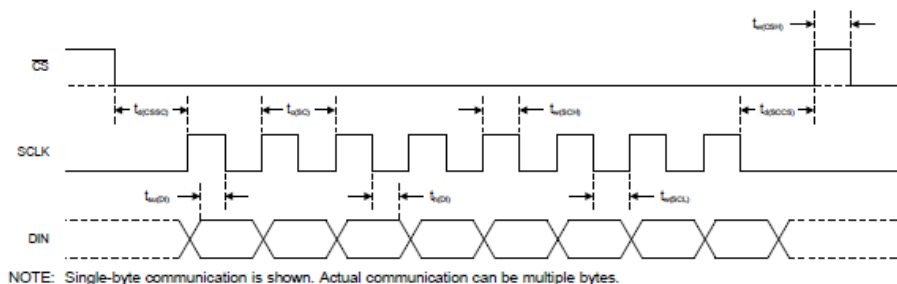


Figure 6 Interface Timing Requirements

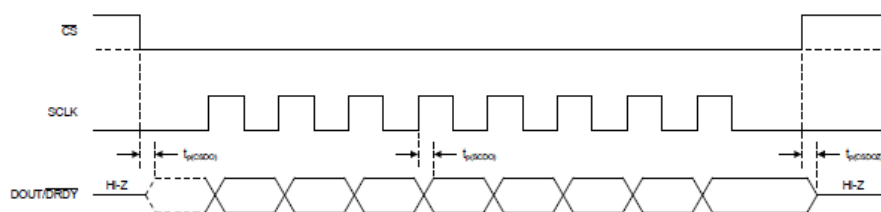


Figure 7 Serial Interface Switching Characteristics



Figure 8 RESET Pin and RESET Command Timing Requirements

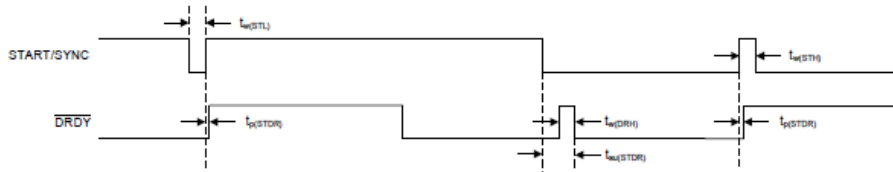


Figure 9 START/SYNC Pin Timing Requirements

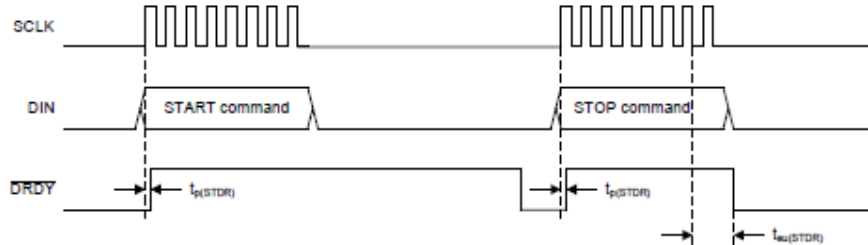


Figure 10 START Command Timing Requirements

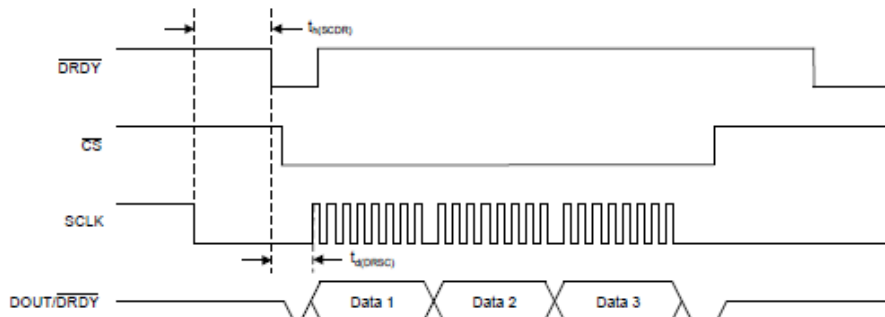


Figure 11 Read Data Direct (Without an RDATA Command) Timing Requirements

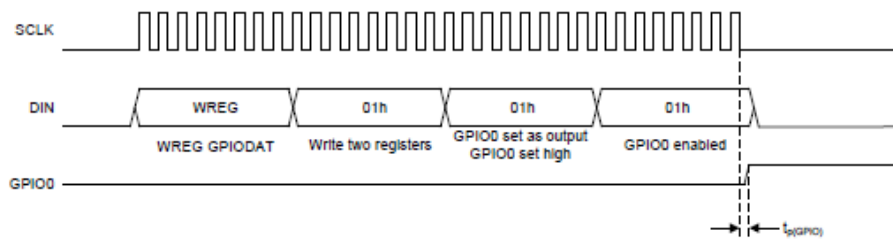


Figure 12 GPIO Switching Characteristics

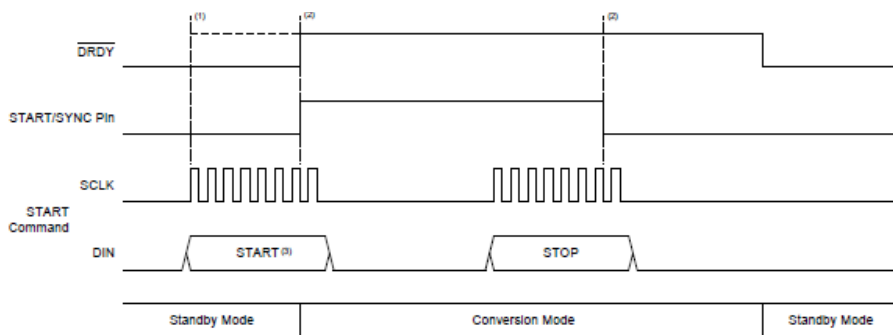


Figure 13 Conversion Start and Stop Timing

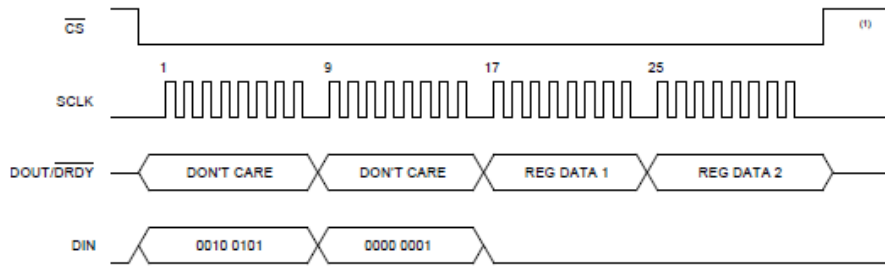


Figure 14 Read Register Sequence

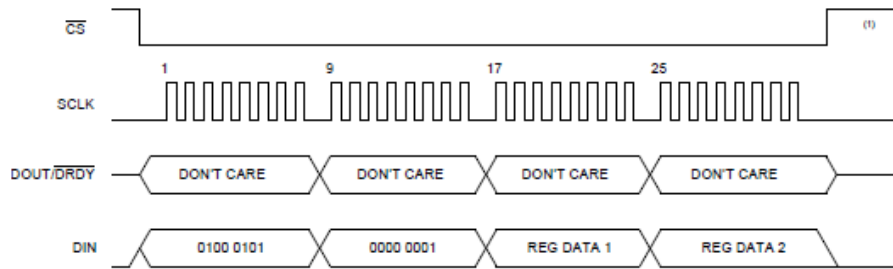


Figure 15 Write Register Sequence

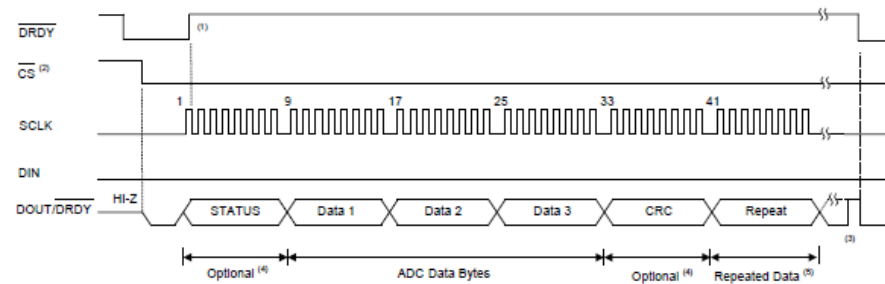


Figure 16 Read Data Direct

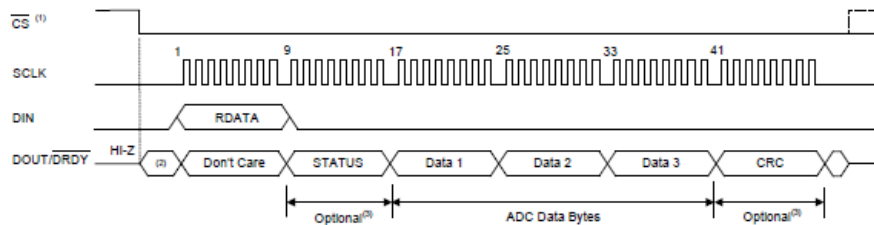


Figure 17 Read Data by Command

Please check the ADS124S06 datasheet for more details, and for a pseudo code example please contact support@varadis.com.

Interface with the HOST

Typical connection with the host is presented in the following figure:



Figure 18: SPI connection with HOST.

IsoSPI communication can be established with a host equipped with isoSPI interface providing bidirectional SPI communications between two isolated devices through a single twisted pair connection. The onboard LTC6820 encodes logic states into signals that are transmitted across an isolation barrier to another LTC6820. The module isoSPI interface is configured as slave, SCK idles low, and latches on falling (2nd) edge.



Figure 19: isoSPI connection with HOST.

isoSPI Demo Circuit Interface

In the following diagram a demo connection with a host using development kits DC1941D isoSPI™ Demo Board and DC2026C, Linduino One Isolated Arduino-Compatible Demonstration Board:

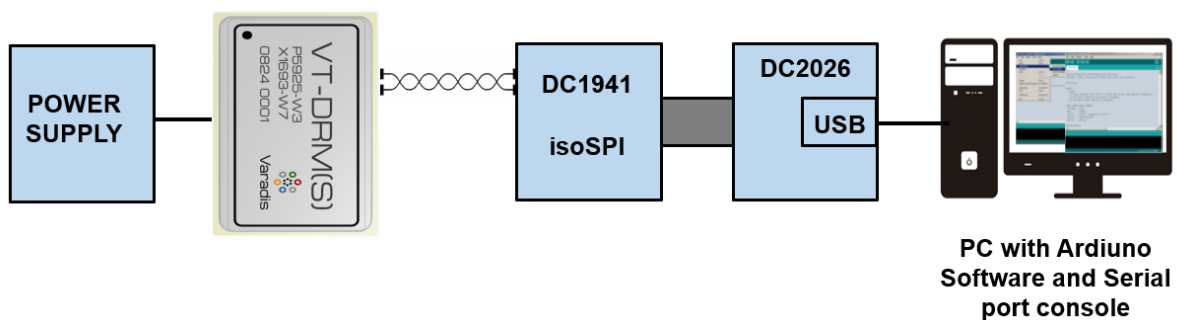


Figure 20: isoSPI example connection with PC.

Radiation Calibration Data

The module is tested in Co-60 field to a total ionising dose of 150 Gy (15 kRad) and dose-rate of 22.6Gy/h (2.26kRad/h). The typical TID level of the module is set to this value, please see Table 4 for details. A higher TID level is possible using a specific mode of operation and shielding. Please contact support@varadis.com for details.

EMP tolerance

The module's ceramic base (PCB ground plane) and metal lid provide a conductive enclosure, protecting the module electronics from incoming electromagnetic energy by creating a Faraday shield. A proper grounding provided by the host is essential for the dissipation of the induced currents and voltages. A single-point ground will minimise the ground loops while a multipoint grounding is effective for high-frequency EMP. We recommend connecting all GND pins to host ground terminal.

Recommended Operating Conditions

VT-DRM(S) module recommended operating conditions are given in Table 3.

Table 3: Recommended Operating Conditions

| Symbol | Parameter | Value | Unit |
|--------|---|---------|------|
| Vdd | Supply voltage, referenced to GND | 3.3 V | V |
| Va | Supply voltage, referenced to GND | 12V | V |
| Din | Serial Data Input | Vdd-0.2 | V |
| CS | Chip Select Input | Vdd-0.2 | V |
| DOUT | Serial Data Output/Data Ready Output | Vdd-0.2 | V |
| SYNC | Synchronization Input | Vdd-0.2 | V |
| SCLK | Serial Clock Input | Vdd-0.2 | V |
| GND | Supply ground | 0 | V |
| Im | Isolated Interface Minus Input/Output | - | V |
| Pp | Isolated Interface Plus Input/Output | - | V |
| T | Ambient operating temperature | 22 | °C |
| ARH | Ambient relative humidity (non-condensed) | < 85 | % |

DC Electrical Characteristics

VT-DRM(S) module DC electrical characteristics are given in Table 4.

Table 4: DC electrical characteristics

| Parameter | Min | Typical | Max |
|----------------------------------|----------------|---------|------|
| Digital supply | 2.7 V | 3.3 V | 3.6V |
| Analog supply | 11V | 12V | 15V |
| Current consumption reading mode | - | 10mA | - |
| Current consumption sense mode | 0 ¹ | 100nA | 30uA |

¹ In case of unpowered module (Va=Vdd=0V) without hi-sense feature (+Gate Bias)

| | | | |
|--|-------|-------------|-------|
| Sensitivity ² 100nm Zero Biased | - | 1.5 mV/Gy | - |
| Sensitivity 100nm +Gate Biased | - | 5.96mV/Gy | - |
| Sensitivity 400nm Zero Biased | - | 0.55 mV/cGy | - |
| Sensitivity 400nm +Gate Biased | - | 130mV/Gy | - |
| TID | 1Rad | 15kRad | - |
| Temperature range | -40 C | 20 C | +85 C |
| Measurement interval | - | 2min | - |

Soldering and Mounting

VT-DRM(S) can be soldered directly on the customer PCB (as SMD), the recommended dimensions for solder pad layout are given in Figure 21.

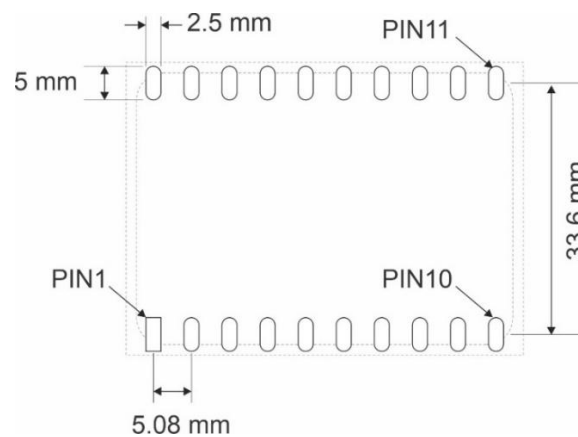


Figure 21: Recommended solder pad layout (top view).

Handling

All modules undergo 100% electrical test and visual inspection immediately prior to shipment. Therefore, all modules should reach the customer in excellent condition. To ensure that the boards remain in this condition, please handle the parts as carefully as possible and observe standard precautions related to ESD sensitive devices.

² The sensitivity decreases with the received dose, the given typical sensitivity is extracted from the linear region (beginning of radiation)

Notes

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